AMENDMENT

In the Claims:

1. (Currently Amended) An apparatus, comprising:

a queue;

a programmable event conditioning logic unit to receive a queue enter signal, a queue exit signal, and a queue not empty signal from the queue, the queue enter signal to be asserted in response to an entry entering the queue, the queue exit signal to be asserted in response to an entry exiting the queue, and the queue not empty signal to indicate that the queue contains at least one entry;

a first counter to increment in response to a first increment event signal delivered by the event ~~selection~~ conditioning logic unit, the first counter to decrement in response to a first decrement event signal delivered by the event ~~selection~~ conditioning logic unit; and

a second counter to increment in response to a second increment event signal delivered by the event ~~selection~~ conditioning logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event ~~selection~~ conditioning logic unit,

wherein assertion of at least one of the second increment event signal and the second decrement event signal is based on a value of the first counter.

2. (Previously Presented) The apparatus of claim 1, the event conditioning logic unit to further receive an inverted version of the queue not empty signal.

3. (Previously Presented) The apparatus of claim 2, further comprising a data register coupled to the first counter.

4. (Previously Presented) The apparatus of claim 3, further comprising a comparator including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the first counter, and the output provided to the event conditioning logic unit.

5. (Previously Presented) The apparatus of claim 4, the event conditioning logic including programmable functions to allow a variety of combinations of the queue enter, queue exit, queue not empty, queue empty, and comparator output signals to serve as increment or decrement events.

6. (Original) The apparatus of claim 5, further comprising a block of registers including a command register and a status register.

7. (Currently Amended) An apparatus, comprising:

a queue;

a programmable event conditioning logic unit to receive a queue enter signal, a queue exit signal, and a queue not empty signal from the queue, the queue enter signal to be asserted in response to an entry entering the queue, the queue exit signal to be asserted in response to an entry exiting the queue, and the queue not empty signal to indicate that the queue contains at least one entry; and

a first counter to increment in response to a first increment event signal delivered by the event ~~selection~~ conditioning logic unit, the first counter to decrement in response to a first decrement event signal delivered by the event ~~selection~~ conditioning logic unit;

a data register coupled to the first counter;

a comparator including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the first counter, and the output provided to the event conditioning logic unit; and

a second counter to increment in response to a second event signal delivered by the event ~~selection~~ conditioning logic unit, the second event signal in response to the comparator output indicating that the first counter value matches the data register value.

8. (Previously Presented) The apparatus of claim 7, the event conditioning logic unit to further receive an inverted version of the queue not empty signal.

9. (Cancelled)

10. (Cancelled)

11. (Previously Presented) The apparatus of claim 8, the event conditioning logic including programmable functions to allow a variety of combinations of the queue enter, queue exit, queue not empty, queue empty, and comparator output signals to serve as increment or decrement events.

12. (Cancelled)

13. (Previously Presented) The apparatus of claim 11, further comprising a block of registers including a command register and a status register.

14. (Currently Amended) A system, comprising:

a processor; and

a system logic device coupled to the processor, the system logic device including

a queue,

a programmable event conditioning logic unit to receive a queue enter signal, a queue exit signal, and a queue not empty signal from the queue, the queue enter signal to be asserted in response to an entry entering the queue, the queue exit signal to be asserted in response to an entry exiting the queue, and the queue not empty signal to indicate that the queue contains at least one entry, and

a first counter to increment in response to a first increment event signal delivered by the event ~~selection~~ conditioning logic unit, the first counter to decrement in response to a first decrement event signal delivered by the event ~~selection~~ conditioning logic unit;

a second counter to increment in response to a second increment event signal delivered by the event ~~selection~~ conditioning logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event ~~selection~~ conditioning logic unit,

wherein assertion of at least one of the second increment event signal and the second decrement event signal is based on a value of the first counter.

15. (Previously Presented) The system of claim 14, the event conditioning

logic unit to further receive an inverted version of the queue not empty signal.

16. (Previously Presented) The system of claim 15, further comprising a data register coupled to the first counter.

17. (Previously Presented) The system of claim 16, the system logic device further including a comparator including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the first counter, and the output provided to the event conditioning logic unit.

18. (Original) The system of claim 17, the event conditioning logic including programmable functions to allow a variety of combinations of the queue enter, queue exit, queue not empty, queue empty, and comparator output signals to serve as increment or decrement events.

19. (Original) The system of claim 18, the system logic device further including a block of registers including a command register and a status register.

20. (Previously Presented) A method, comprising:

delivering a queue enter signal, a queue exit signal, and a queue not empty signal to a programmable event conditioning logic unit, the queue enter signal to be asserted in response to an entry entering a queue, the queue exit signal to be asserted in response to an entry exiting a queue, and the queue not empty signal to indicate that queue contains at least one entry;

asserting a first increment event signal in response to an occurrence of a first programmable combination of the queue enter signal, the queue exit signal, and the queue not empty signal;

incrementing a first counter in response to the assertion of the first increment event signal;

asserting a first decrement event signal in response to an occurrence of a second programmable combination of the queue enter signal, the queue exit signal, and the queue not empty signal;

decrementing the first counter in response to the assertion of the first decrement event signal;

asserting a second event signal; and

incrementing a second counter in response to the assertion of the second event signal, the second event signal asserted in response to the first counter matching a threshold value.

21. (Previously Presented) The method of claim 20, further comprising storing the first counter value in a data register.

22. (Previously Presented) The method of claim 20, further comprising comparing the first counter value with a data register value, the data register value equal to the threshold value.

23. (Previously Presented) The apparatus of claim 7, the first increment event signal issued in response to the assertion of the queue not empty signal.

24. (Previously Presented) The apparatus of claim 7, the first decrement event signal issued in response to the assertion of the queue exit signal.

25. (Previously Presented) The apparatus of claim 7, the data register programmable with a threshold level value.